WE CLAIM:

1. A semiconductor storage apparatus to be coupled with a system bus to receive a write request accompanied with first and second blocks of data, comprising;

a plurality of nonvolatile semiconductor memories which store said first and second blocks of data therein; and

a control means to be coupled with said system bus, and coupled with said plurality of nonvolatile semiconductor memories,

wherein said control means sends a first erase command to one of said plurality of nonvolatile semiconductor memories to initiate a first internal erase operation of data within said one of said plurality of nonvolatile semiconductor memories, and

wherein, after said first erase command has been sent, said control means sends a second erase command to another of said plurality of nonvolatile semiconductor memories, different from said one of said plurality of nonvolatile semiconductor memories to which said first erase command was sent and which is under said first internal erase operation, to initiate a second internal erase operation of data within said other of said plurality of nonvolatile semiconductor memories.

2. A semiconductor storage apparatus according to claim 1, farther comprising:

a buffer memory, coupled commonly with said plurality of nonvolatile semiconductor memories, which holds said first and second blocks of data as write data to be written into said plurality of nonvolatile semiconductor memories,

wherein said control means responds to said write request, carries out read operations of said first and second blocks of data as said write data from said buffer memory and carries out write operations of said first and second blocks of data as said write data read out from said buffer memory into said plurality of nonvolatile semiconductor memories, wherein said write operations into said plurality of nonvolatile semiconductor memories are controlled by sending a first write command from said control means to one of said plurality of nonvolatile semiconductor memories and by sending a second write command from said control means to another of said plurality of nonvolatile semiconductor memories different from said one to which said first write command has been sent and which is under a write operation responsive to said first write command.

3. A semiconductor storage apparatus according to claim 1, wherein each of said plurality of nonvolatile semiconductor memories is comprised of a flash memory semiconductor chip.

4. A semiconductor storage apparatus according to claim 2, wherein each of said plurality of nonvolatile semiconductor memories is comprised of a flash memory semiconductor chip.

5. A semiconductor storage apparatus according to claim 2, wherein said buffer memory has a storage memory capacity corresponding to a plurality of sectors in units of 512 bytes which is a sector capacity of a standard disk.

6. A semiconductor storage apparatus according to claim 1, wherein said control means includes a processor.

7. A semiconductor storage apparatus according to claim 2, wherein said control means includes a processor

8. A semiconductor storage apparatus according to claim 1, wherein said control means further includes an address controller.

9. A semiconductor storage apparatus according to claim 2, wherein said control means further includes an address controller,

10. A semiconductor storage apparatus according to claim 1, wherein each of said plurality of nonvolatile semiconductor memories is comprised of a flash memory semiconductor chip, and wherein said buffer memory has a storage memory capacity corresponding to a plurality of sectors in units of 512 bytes which is a sector capacity of a standard disk.

11. A semiconductor storage apparatus according to claim 2,

wherein each of said plurality of nonvolatile semiconductor memories is comprised of a flash memory semiconductor chip, and

wherein said buffer memory has a storage memory capacity corresponding to a plurality of sectors in units of 512 byte which is a sector capacity of a standard disk.

12. A semiconductor storage apparatus according to claim 10, wherein said control means includes a processor.

13. A. semiconductor storage apparatus according to claim 11, wherein said control means includes a processor.

14. A semiconductor storage apparatus according to claim 10, wherein said control means further includes an address controller.

15. A semiconductor storage apparatus according to claim 11, wherein said control means further includes an address controller.